5701

Super-GLU Gate Array Technical Specification

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The Super-GLU (General Logic Unit) is a gate array designed to interface a 68000 Microprocessor with the Ensoniq ESP Digital Signal Processor and with an OTIS chip. In addition, the gate array includes circuitry to interface the OTIS multiplexed address/data bus with static memory chips (RAMs or ROMs). This chip can be used in all OTIS-based products including samplers, synthesizers, pianos, etc.

The gate array provides these basic functions:

1) 68000 to ESP interface:
The address and data from the Microprocessor must be multiplexed together to communicate with the ESP. In addition, a DTACK signal must be generated for the 68000.

2) 68000 to OTIS interface:
The address and data from the Microprocessor must be isolated from the sound bus during an OTIS access of sound memory and passed through during a processor access of the OTIS registers or sound memory. In addition, when the sample word width is less than 16 bits, the unused bits should be pulled low on a processor read of sound memory.

3) OTIS interface to static memory:
The multiplexed address/data from the OTIS must be demultiplexed and latched for use with static memory. In addition, when the sample word width is less than 16 bits, the unused bits must be pulled low on an OTIS read of sound memory. When 12-bit mode is selected and byte-wide memories are being used, the appropriate nybble (upper or lower) of sound memory must be sent to the low order data lines of OTIS.

4.) Clock Generator:
A crystal oscillator and divider are provided for use with a 20 MHz crystal to produce the 10 MHz output clock for the system. A second crystal oscillator and divider is provided for use with a 16 MHz crystal to produce an 8 MHz clock for use in products with disk drives.

The following is a list of pins and their functions:

Pin	Type	Description	Function
+5	IN	Supply	
GND	IN	Supply	
D15	I/O (T.S.)	MPU Data Bus	
D14	I/O (T.S.)		D15-D0 to/from OTIS or Sound Memory
D13	I/O (T.S.)		D7-D0 to/from ESP
D12	I/O (T.S.)		
D11	I/O (T.S.)		Data transfers gated with /UDBEN, /LDBEN, /ESP
D10	I/O (T.S.)		/DBUS and R/W. Assumes the DBEN lines are
D9	I/O (T.S.)		already gated with the appropriate chip selects
D8	I/O (T.S.)		(i.e. the OTIS chip select and the Sound Memory
D7	I/O (T.S.)		chip select)
D6	I/O (T.S.)		
D5	I/O (T.S.)		
D4	I/O (T.S.)		Low order bits will be pulled low on a processor
D3	I/O (T.S.)		read of Sound Memory depending on the sample
D2	I/O (T.S.)		word width
D1	I/O (T.S.)		
D0	I/O (T S.)		

A8	IN	MPU Address Bus
A7	IN	A4 - A1 to OTIS or Sound Memory
A6	IN	A8 - A1 to ESP
A5	IN	
A4	IN	
A3	IN	
A2	IN	
A1	IN	
R/W	IN	MPU Read/Write line
/UDBEN	IN	Upper Data Bus enable
/LDBEN	IN	Lower Data Bus enable
/ESP	IN	ESP Chip Select
/DTACK	OUT (O.C.)	DTACK for ESP
/RAS	IN	OTIS /RAS output
/CAS	IN	OTIS /CAS output
/DBUS	IN	OTIS sound bus arbitration clock
A8/D7	I/O (T.S.)	Muxed Address/Data for ESP
A7/D6	I/O (T.S.)	MPU A8 - A1 to ESP
A6/D5	I/O (T.S.)	MPU D7 - D0 to/from ESP
A5/D4	I/O (T.S.)	
A4/D3	I/O (T.S.)	Multiplexing controlled by /ESP chip select
A3/D2	I/O (T.S.)	
A2/D1	I/O (T.S.)	
A1/D0	I/O (T.S.)	
LA19	OUT (T.S.)	Latched Address from OTIS to static Sound Memory
LA18	OUT (T.S.)	
LA17	OUT (T.S.)	OTIS addresses latched by fall of ~~/CAS~~ /RAS, outputs
LA16	OUT (T.S.)	enabled by /DBUS
LA15	OUT (T.S.)	
LA14	OUT (T.S.)	
LA13	OUT (T.S.)	
LA12	OUT (T.S.)	
LA11	OUT (T.S.)	
LA10	OUT (T.S.)	
LA9	OUT (T.S.)	
LA8	OUT (T.S.)	
LA7	OUT (T.S.)	
LA6	OUT (T.S.)	
LA5	OUT (T.S.)	
LA4	OUT (T.S.)	
DA19	I/O (T.S.)	OTIS Muxed Address/Data /RAS
DA18	I/O (T.S.)	
DA17	I/O (T.S.)	Latched into LA19 - LA4 on fall of ~~/CAS~~ /RAS
DA16	I/O (T.S.)	Lower data bits to OTIS forced low by /DBUS
DA15	I/O (T.S.)	depending on sample word width
DA14	I/O (T.S.)	
DA13	I/O (T.S.)	
DA12	I/O (T.S.)	
DA11	I/O (T.S.)	
DA10	I/O (T.S.)	
DA9	I/O (T.S.)	
DA8	I/O (T.S.)	
DA7	I/O (T.S.)	
DA6	I/O (T.S.)	

DA5	I/O (T.S.)	
DA4	I/O (T.S.)	
DA3	OUT (T.S.)	OTIS low order address
DA2	OUT (T.S.)	
DA1	OUT (T.S.)	Passes MPU address to OTIS or Sound Memory
DA0	OUT (T.S.)	
DA11H	IN	Nybble inputs for 12-bit systems
DA10H	IN	
DA9H	IN	
DA8H	IN	Passes upper or lower nybble of Sound Memory
DA11L	IN	to OTIS (DA11-DA8)
DA10L	IN	
DA9L	IN	
DA8L	IN	
M1	IN	Sample word width select MSB
M0	IN	Sample word width select LSB
/NYB	IN	Selects nybble mode for 12-bit systems
20MI	IN	20 MHz crystal connection
20MO	OUT	20 MHz crystal connection
10M	OUT	Buffered 10 MHz output clock
16MI	IN	16 MHz crystal connection
16MO	OUT	16 MHz crystal connection
8M	OUT	Buffered 8 MHz output clock

Total: 99 pins (assumes three supply pins and three ground pins)

The functional blocks operate in the following manner:

Data is transferred between the 68000 and OTIS or Sound Memory via D15-D0 and DA19-DA4. R/W controls the direction of data transfer and all tranfers are gated with /DBUS which indicates when the shared bus is available. /UDBEN and /LDBEN allow either upper or lower bytes or words to be transferred. Depending on the sample word width selection, the lower 8,4 or 3 bits to the 68000 can be forced low when the processor is reading sound memory.

The low order address of the processor (A4-A1) is sent to OTIS (DA3-DA0) and the Sound Memory whenever either /UDBEN or /LDBEN are low and /DBUS is high. This allows the 68000 to select the appropriate OTIS register or address low order Sound Memory.

Address information from the OTIS chip, supplied on DA19-DA4, is latched at the fall of /RAS to keep it stable during the entire OTIS sound memory access. The latched address outputs are enabled when /DBUS is low, indicating an OTIS memory access. By floating these outputs when /DBUS is high, it is possible to share this bus, which may be useful in future products.

Depending on the sample word width, the lower 8,4 or 3 data bits to OTIS (on the DA lines) can be forced low on an OTIS read of sound memory. When /NYB is tied low and 12-bit mode is selected, data nybbles supplied on DA11H-DA8H and DA11L-DA8L are routed to DA11-DA8 when /DBUS is low and /CAS is low. This function is normally only used in systems with 12-bit sound samples and byte-wide memory chips. One set of memory chips provide the upper byte of the sample word, while the Nybble memory chip provides two nybbles. The upper byte, along with one of the nybbles, forms the 12-bit word. The desired nybble is selected by the state of LA19. This is simply a convenient method of packing 12-bit sample words into less memory chips.

Data is transferred between the 68000 and ESP via D7-D0 and A8/D7-A1/D0. R/W controls the direction of data transfers and all transfers are gated with /ESP. When /ESP is high, A8-A1 are sent out

A8/D7-A1/D0. When /ESP falls, the address information is turned off and D7-D0 are sent to A8/D7-A1/D0. This accomplishes the multiplexing necessary for the ESP bus interface. The address outputs must meet the hold time requirements of the ESP chip. /ESP is reflected back to the processor by an open-collector buffer in order to provide a /DTACK signal for the 68000. This DTACK timing must be consistent with the ESP and 68000 bus timing.

M1 and M0, the sample word width bits, are used to select the desired number of bits for the sample memory. The possible selections are 16-bits, 13-bits, 12-bits and 8-bits. Depending on the word width selected, some or all of the low order data lines to both the 68000 and OTIS are forced low during a sound memory read. Whenever /CAS is low, this indicates that either the 68000 is accessing sound memory or OTIS is accessing sound memory and the appropriate data lines should be pulled low on a read.

M1	M0	Mode	MPU lines pulled low	OTIS lines pulled low
1	1	16-bit	none	none
1	0	13-bit	D2-D0	DA6-DA4
0	1	12-bit	D3-D0	DA7-DA4
0	0	8-bit	D7-D0	DA11-DA4

The crystal oscillators are standard cells and their outputs are divided by two using a flip-flop to insure 50% duty cycles.

Note that this design assumes that the low order address outputs from OTIS (DA3-DA0) do not go into Tri-State at the fall of /CAS during an OTIS sound memory access.

The following schematics show one possible implementation.

ON SUPERCLU

TIE M1 TO GND

CONNECT M0 TO

$\overline{CS}$ FOR 8-BIT SOUNDS

WHEN M0 IS LOW,

8 BIT MODE IS

SELECTED, LOWER BITS

ARE PULLED LOW ON

READ.